

## *FX/2800 Standards-Based Supercomputer*



Miata Courtesy of Mazda Motor Company

*Alliant's Most Flexible,  
Standards-Based  
Supercomputer*

# FX/2800 Standards-Based Supercomputer

## FX/2800 Highlights

- Up to 28 64-bit RISC processors for computation, graphics and I/O tasks that can be dynamically assigned based on changing user workloads.
- PAX compatible.
- Field expandable processors, memory and I/O subsystems.
- Up to 1GB shared memory and 4MB of cache memory accessed via a 1.28GB/sec. crossbar interconnect.
- Parallel optimizing compilers for standard languages (Fortran, C, Ada®).
- Parallel implementation of PHIGS/PHIGS+ within the X11™ windowing environment.
- Symmetric multiprocessing (SMP) implementation of UNIX® with extensive multithreading for maximum throughput.
- FX/RT™ real-time execution environment co-resident with standard UNIX.
- Shared memory communication between processors for high-speed interprocess communication.

- Network services: Ethernet™ with TCP/IP and DECnet™, NFS™, NCS®, NQS™, X Window System, Version 11™ and UltraNet®.
- High-resolution (1280x1024) full-color display (8-bit, 16-bit, 24-bit and 48-bit) with hardware-based Z-buffering.
- Multi-channel graphics output and multiple visualization displays supported on single system.
- Alliant's VISEEDGE™ and VIA-CL™ visualization tools for rapid display of graphics data without graphics programming.
- Up to 16 high-speed VME I/O channels.
- Support for parallel I/O via disk striping.
- Multithreaded I/O drivers provide high throughput.
- 90GB+ of on line storage.
- Backup provided via high-capacity 8mm helical scan devices, with optional 9-track tape subsystems also available.

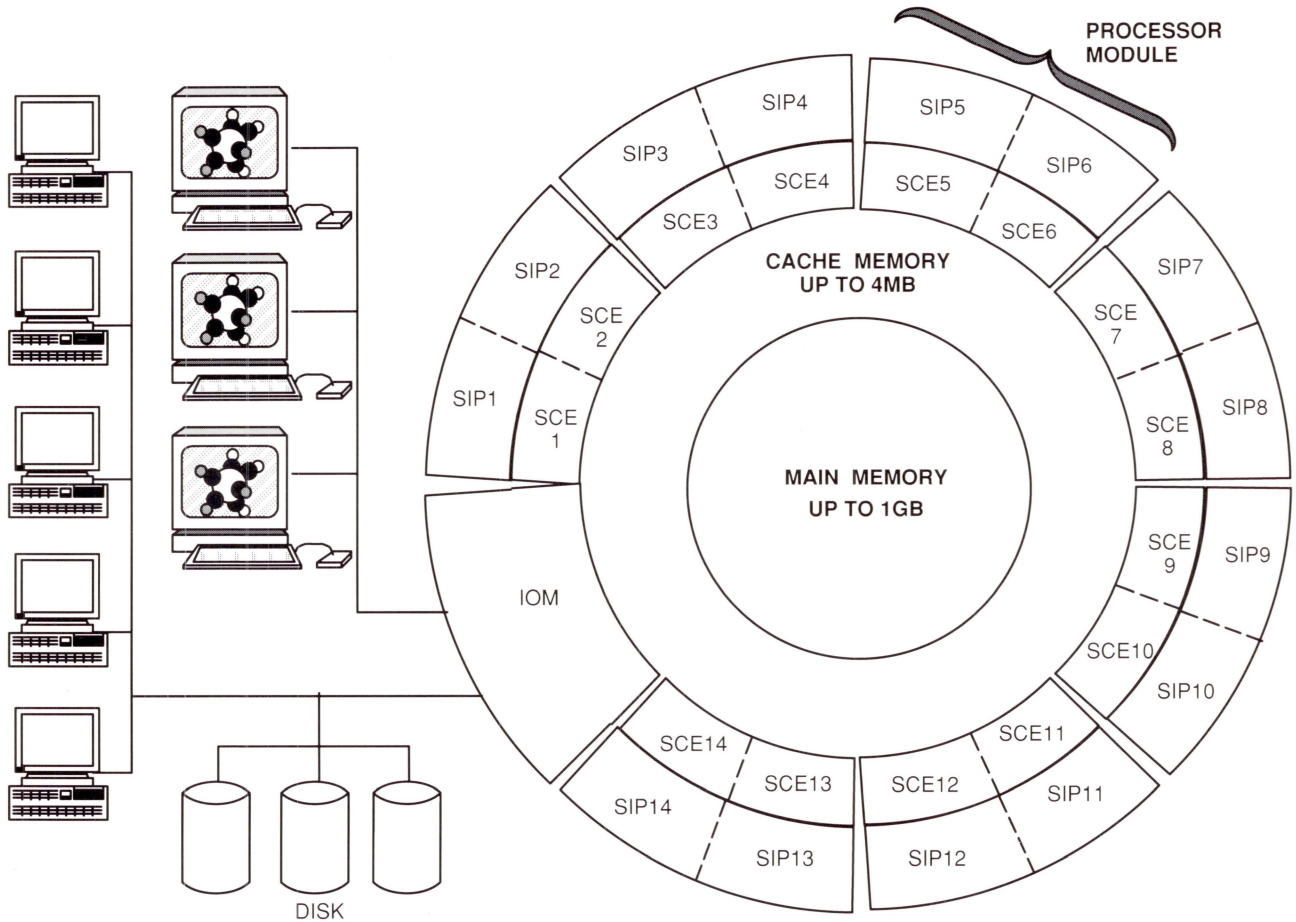
## The FX/2800 Standards-Based Supercomputer

With supercomputer performance of over 1.1 GFLOPS, the FX/2800™ uses parallel processing, multiprocessing and visualization, simultaneously, to offer scientific and engineering users the widest array of computational resources available.

The FX/2800 family of parallel supercomputers can be configured with up to 28 64-bit RISC processors, arranged as 14 Super Computational Elements (SCEs) for parallel processing of large compute intensive tasks, and 14 Super Interactive Processors (SIPs) for multiprocessing serial compute jobs, executing system tasks, I/O and 3-D graphics processing.

A single Processor Module (PM) contains four Intel i860™ processors, arranged as 2 SCEs and 2 SIPs. Up to seven (field-installable) PMs are supported in the FX/2800, allowing users to expand their systems incrementally as their needs expand. An additional SIP is combined with two 20MB/sec. I/O channel interfaces to form an I/O module (IOM).

SYSTEM PERFORMANCE
Up to 1.12 double-precision peak GFLOPS
Up to 672 double-precision Whetstone MIPS (24 MWhetstones per processor)
Up to 1148 Dhrystone MIPS (41K Dhrystone MIPS per processor, V1.1)
11 MFLOPS per processor on 100x100 LINPACK
Up to 720 MFLOPS on 1000x1000 LINPACK



The FX/2800 architecture offers a variety of resources designed to meet the varying needs of high performance users.

### Standards-Based Processors

FX/2800 processors are based on the 64-bit Intel i860 processor, combined with Alliant's Concurrency Control Architecture.

The integer core of each processor is based on RISC (Reduced Instruction Set Computer) technology. Simplicity of design gives RISC architectures the capability to outperform conventional architectures that use complex instruction sets. The reduced instruction set allows the average instruction to execute in far fewer clock cycles - typically a single cycle - thereby maximizing system performance.

Each processor consists of multiple functional units working in parallel - the RISC integer core, floating-point multiplier and floating-point adder, and a 3-D graphics unit. This permits the execution of "superscalar" operations of up to three instructions in a single clock cycle - ie., integer, or graphics, floating-point add and floating-point multiply - providing true instruction-level parallelism.

The floating-point unit can execute both scalar (non-pipelined) and vector (pipelined) variants of floating-point instructions with high scalar throughput. The pipelined mode allows Alliant's compilers to efficiently optimize applications that have been tuned for traditional vector architectures. The combination of "superscalar" operations with pipelining results in a unique Alliant compiler technique known as "RISC vectorization".

## ***FX/2800 Standards-Based Supercomputer***

### **Parallel Clusters for Maximum Speed**

The FX/2800 provides high single job computational performance by grouping up to 14 SCEs together into a parallel cluster. Up to six clusters of varying size can be running several jobs in parallel simultaneously. In addition, SCEs can run independently on separate user jobs. The amount of time the SCEs spend as part of a cluster can be optimized via the Concentrix® scheduler. This achieves maximum user interactivity and job throughput. The Concentrix operating system scheduler automatically switches between modes to provide optimum use of resources at all times. Alliant's parallel compilers automatically generate code for parallel execution, transparently to the user.

The synchronization of the processors in a cluster is controlled in hardware for maximum efficiency. The Concentrix operating system treats the processors in the cluster as a single computational resource. Unlike process-based or "threads-based" multiprocessing systems, which allocate additional processors via operating system-controlled queues, processors in the parallel cluster are immediately available to a parallel job, without the intervention of the operating system. This ensures minimum latency in initiating loop-level parallel processing required for rapid execution of engineering and scientific programs.

### **Multiprocessing for Maximum Throughput**

In addition to the SCEs, the FX/2800 provides up to 14 Super Interactive Processors (SIPs). Development activities such as compiling, debugging, and editing are performed by the SIPs, giving each user the equivalent of a very responsive high-speed super workstation with 41 MIPS (Dhrystones) and 24 MIPS (double precision Whetstones) of scalar processing power. The SIPs also execute operating system tasks such as paging and swapping, file system management, networking, and I/O, as well as parallel 3-D graphics.

### **Simultaneous Computation and Graphics**

The large number of processors available for both computation and graphics allows users to view and interact with a simulation as it is being calculated, or interactively view large data sets that have previously been calculated while generating additional data sets in the background.

Users can easily add processors for computation and graphics, or vary the allocation of processors based on changing requirements.

### **Parallel PHIGS/PHIGS+ in the X11 Environment**

The FX/2800 provides a parallel implementation of PHIGS/PHIGS+ transparently to the user. PHIGS/PHIGS+ applications execute in the X11 windowing environment, providing 3-D applications portability and a standard windowing library for user interface design and input. The X11 client/server connection is implemented via shared memory IPC (Interprocess Communication) for maximum performance.

### **High-Speed Graphics Processing**

All floating point-intensive geometric operations for PHIGS/PHIGS+ applications - such as 3-D transformations, shading, clipping, tessellation and lighting models - are handled directly and efficiently by the SIPs.

Multiple SIPs can be combined in clusters to provide higher performance geometry processing via parallelism. This approach often yields higher performance than that provided by rigid geometry pipelines implemented in special-purpose hardware, while providing maximum user flexibility in configuring the appropriate number of processors to compute and graphics tasks.

For non PHIGS/PHIGS+ compute-intensive graphics applications such as image processing, and advanced rendering applications such as volume rendering and photorealistic rendering, the user can configure clusters of SCEs to provide the high performance required to approach real-time image generation.

### High Performance Memory System

The FX/2800 computational resources are connected to the system's memory subsystem through a 16 x 8 crossbar switch. This interconnect provides a bandwidth of 1.28GB/sec. to the system's, shared global cache and main memory. Cache Memory modules contain 512KB of high speed static RAM. Up to eight cache modules, or 4MB, can be configured into an FX/2800 system.

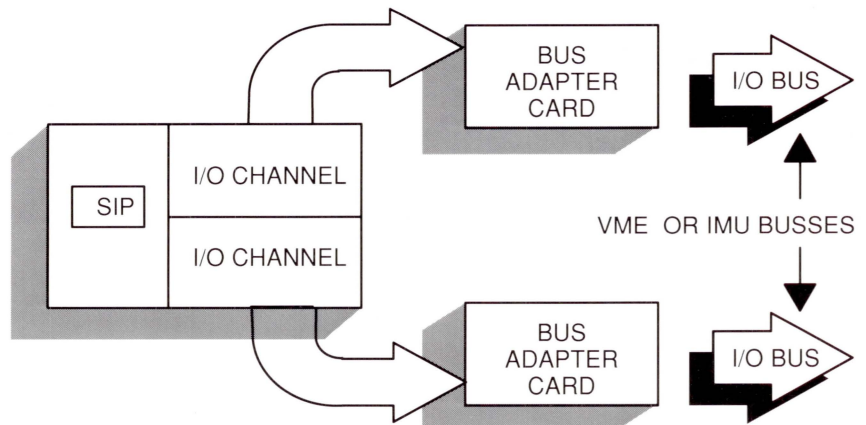
The caches are connected via a 72 bit wide bus structure to main memory. The aggregate bandwidth across this bus is 640MB/sec. Memory modules contain 64MB of ECC RAM. Up to 16 memory modules, or 1GB of physical memory, can be configured into a FX/2800 system. Virtual memory addressing is 4GB.

### Distributed I/O

The FX/2800 is ideally suited as a network file and compute server for workstations, VAX™ systems, and as a front-end or back-end to CRAY™ supercomputers. Multiple high-speed VME channels support large capacity disk storage, tape backup devices and high-speed network interfaces.

Each FX/2800 I/O Module (IOM) contains a single SIP processor for I/O control. This SIP is also available to the overall pool of SIP processors when not engaged in I/O activity.

Each IOM supports up to two I/O channels that provide a maximum transfer rate of 40MB/sec. peak out of memory and 25MB/sec. peak into memory. An I/O channel can be used for either VME I/O or image memory subsystems.



The FX/2800 I/O module provides two I/O channels that can be connected to either VME or IMU adapters.

Multiple IOMs can be used to provide multiple VME channels and/or multiple image memory subsystems. PMs and IOMs can be configured to match user requirements, up to a maximum of eight boards total.

Due to extensive multi-threading in the operating system, I/O transfers can occur on multiple channels simultaneously and overlap with the execution of related operating system tasks such as file management.

Large files can be interleaved across multiple disks and controllers in a contiguous fashion via "disk striping", transparently to the user. Striped files are accessed by several disk controllers working in parallel, resulting in enhanced disk throughput.

### Image Memory Subsystem

The optional image memory subsystem provides tightly-coupled image display hardware for real-time visualization output.

The FX/2800 supports multiple simultaneous high-resolution displays for applications such as multi-channel simulation and multi-user visualization environments. Up to four image memory subsystems are supported with each subsystem supporting up to four displays.

Each display consists of an Image Memory Unit (IMU) and optional Z-buffer Memory Unit (ZMU) with a 19" non-interlaced 60 Hz monitor. The IMU provides the frame buffer memory along with custom VLSI drawing processors for low-level graphics operations. The 1280x1024 bit frame buffer memory is configurable for both 8-bit (pseudo-color) and 24-bit (true color) applications, including 8-bit and 24-bit double-buffering for smooth animation.

The IMU drawing processors support direct hardware execution of interpolated vectors, smooth shaded patches, rectangle fills, block moves, image transfers and read/write masks. The ZMU provides an additional 1280x1024x16 bits of frame memory for hardware-based Z-buffering.

The fiber-optic RGB option allows the display, keyboard and mouse to be placed up to 1000 feet (300 meters) from the main system cabinet. Other display options include an RGB-to-NTSC/PAL converter for video production, and a 3-D stereoscopic display system.

## ***FX/2800 Standards-Based Supercomputer***

### **Powerful Visualization Tools**

Alliant's powerful visualization tools allow non-programmers to visualize their engineering and scientific data in a minimum amount of time.

VIA-CL is a set of visualization algorithms that help users locate and extract features of interest in their 3-D data. For example, VIA-CL identifies isopotential surfaces from scalar field results, streamlines and topology from vector fields, and tensor field lines from tensor fields.

The VISEEDGE package is an interactive 3-D viewer for geometric models and data. It provides a range of menu-driven, easy-to-use graphics capabilities including dynamic 3-D rotations, various rendering modes, lighting, color coding according to analysis value and animation. VISEEDGE allows you to visualize the output of your simulations – such as those produced by ANSYS®, MSC/NASTRAN and ARC3D - in 3-D under interactive user control. VISEEDGE is also used to view the visualization objects identified by VIA-CL.

### **Parallel Compilers**

Alliant's compilers maximize the efficiency of generated code with a minimum of user intervention. Alliant's FX/Fortran™ and FX/C™ compilers form the core of the PAX standard for i860-based platforms and are therefore also available on other PAX-standard systems. Through the use of a common calling convention, routines written in any of the FX/ Series™ languages can call each other directly and share data.

FX/Fortran is an ANSI-standard optimizing compiler with VAX/VMS™ extensions. It automatically detects the potential for parallel processing in standard Fortran

code. Typical code constructs optimized by FX/Fortran for parallel execution include multiply-nested DO loops (with and without data dependencies); DO-WHILE and IF-GOTO loops; array operations within a loop; matrix multiplication; and linear recurrence relations.

The optional Fortran Automatic Structuring Tool (FAST) automatically structures Fortran programs for parallelism in outer loops. FAST's use of leading-edge inter-procedural analysis techniques results in dramatic programmer productivity while obtaining high performance from existing codes.

The FX/C compiler is compatible with the draft ANSI standard, and shares a common optimizer and code generator with FX/Fortran. It provides for automatic parallel execution of code constructs including FOR loops with IF, IF-ELSE, IF-ELSE-IF-ELSE, and SWITCH; loops with multidimensional array as argument; loops with array of structure; and loops with array of pointer.

The FX/Ada™ compiler has been validated by the U.S. Department of Defense and supports transparent parallel tasking across multiple processors. Ada bindings are provided for the FX/RT real-time execution environment. FX/Ada also includes standard Ada tools for library management, program creation and maintenance, and debugging.

### **Parallel Libraries**

All languages have access to the optional Alliant Scientific Libraries, a set of highly-tuned mathematical routines for linear algebra operations, signal processing, and other scientific functions. A set of Cray compatible mathematics routines is also available.

Alliant also offers the CLASSpack products from KAI and the EXSL (EXtremely large system SoLver) out-of-core solver for efficiently solving systems of equations that are typically larger than 1000x1000 in size. Third-party packages such as Math Advantage®, IMSL™ and NAG are also available for FX/ Series systems.

### **Concentrix Operating System**

The Concentrix operating system is a symmetric multiprocessing implementation of UNIX with extensions for parallel supercomputing. The Concentrix scheduler allows the system administrator to configure the mix of individual SCEs, SIPs and parallel clusters for changing user environments in order to maximize user interactivity and job throughput.

Concentrix provides many of the services required in large multi-user environments, including the NQS batch system and system resource accounting facilities. For real-time applications, Concentrix supports the FX/RT co-resident real-time executive. FX/RT creates a real-time execution environment that retains access to the full UNIX environment. This includes support for priority-driven, preemptive scheduling; process memory residency; shared physical and paged data regions; semaphore-based process synchronization; asynchronous event handling; and Ada-generated parallel tasking.

Alliant is committed to UNIX standards and has announced its intention to support UNIX System V.4 as part of the PAX standard.

### **Network Supercomputing**

Alliant's networking software products allow easy integration into existing workstation, VAX and Cray environments. The ANSR™ (Alliant Network Supercomputing Resources) product family includes support for Ethernet with TCP/IP and DECnet, the Network File System (NFS), Network Computing System (NCS), Network Queuing System (NQS), the UltraNet network and the X Window System, Version 11. Batch jobs can be easily submitted to Alliant systems via a DECnet batch facility for VAX environments, and the NQS facility for Cray UNICOS™ environments. Support for LAT Host Services allows access to Alliant systems and attached printers from terminals connected to a LAT terminal server.

### **VAX/VMS Integration**

A range of integration tools gives VAX users immediate access to the power of Alliant supercomputers. These include a VAX-compatible Fortran compiler; A Digital Command Language (DCL™) interpreter and an EDT-like editor. A third-party VAX-TPU-compatible editor is also available.

### **Peripheral Support and Expansion**

Alliant peripherals include disk and tape subsystems, terminals and printers, and local area networking products. The FX/2800 supports disk farms through multiple I/O channels and disk striping, innovative packaging technology and latest high-density disk drives.

### **System Expansion**

The FX/2800 is easily expandable in the field. As user requirements increase, additional processors, caches and memory modules, are simply added to the system cabinet. Existing software runs unmodified on the expanded system and takes advantage of all installed processors. The addition of display hardware allows utilization of the inherent graphics additions capabilities.

### **Reliability and Maintainability**

Many built-in features ensure data integrity and make the FX/2800 reliable and easy to maintain. Error Checking and Correction (ECC) is used extensively in the memory system. Multiple diagnostic processors include self-test and error logging.

An independent system diagnostic bus and stand-alone diagnostic software allow fault isolation to occur with only a fraction of the hardware operational. The system supports both local and remote fault diagnosis and system reconfiguration.

The modular design of the FX/2800 enhances system availability. Elements such as PMs and IOMs can be logically disconnected from the system, allowing operation to resume quickly after a failure.

### **The Alliant Applications Library**

Alliant's growing supercomputer applications library contains more than 200 of the most respected engineering and scientific software packages. Alliant maintains in-house teams of scientists, engineers and numerical analysis experts to help application developers take advantage of the latest parallel techniques and algorithms.

# FX/2800 Standards-Based Supercomputer

## MACHINE ARCHITECTURE

### General

Symmetric multiprocessor  
Shared memory

### Super Computational Elements (SCEs)

Up to 14 per system  
64-bit RISC technology

### Super Interactive Processors (SIPs)

Up to 14 per system  
64-bit RISC technology

### Instruction Set

Scalar Integer  
Scalar Floating Point (IEEE Standard)  
Pipelined (Vector)  
Concurrency Control

## VIRTUAL ADDRESS SPACE

4GB  
4KB page size

## MEMORY SYSTEM

Cache size 512KB per module,  
4MB max

Processor to Cache Bandwidth:  
1.28GB/sec.

Maximum Physical Memory: 1GB  
Interleaving: 16-way on a single board  
Memory Bus Bandwidth: 640MB/sec.

## I/O SYSTEM

Up to 16 VME (IEEE 1014) or Image  
Memory subsystems

## Disk and Tapes

Dual 8" SMD Winchester Disks  
Max. Storage = 800MB formatted per  
drive (greater than 90GB max per  
system)

50 IPS, 3200 1600/6250BPI  
125 IPS, 800/1600/6250 BPI  
Exabyte 8mm tape drive  
Storage = 2GB/cartridge  
Transfer Rate = 246KB/sec.

## DISPLAY SPECIFICATIONS

Monitor: 19 inch color, 60 Hz  
non-interlaced  
Resolution: 1280x1024  
Frame Buffer: 24 planes  
Double-Buffering: 8-bits (standard) 24-bits  
(optional)  
Distance from system unit:  
50 feet (standard) 1000 feet (optional)

## ENVIRONMENTAL

### Safety Standards Compliance

UL478  
CSACS22.2  
IEC 950  
EMC  
FCC Class A, VDE Class A

### Power

System Cabinet  
US: 120/208V, 3-phase 30A/phase Intl:  
220-240/380-415V, 3-phase,  
32A/phase

I/O Expansion Cabinet  
U.S. 208V, 3-wire 30A  
Intl: 220/240V 3-wire 32A

### Heat output

System Cabinet  
Min: 4733W (16,150 BTU/hr.)  
Max: 7930W (27,050 BTU/hr.)  
I/O Expansion Cabinet  
Max: 3960W (13,500 BTU/hr.)

### Cabinet Dimensions

System Cabinet  
width - 74.9 cm (29.5 in.)  
height - 110.5 cm (43.5 in.)  
depth - 85.8 cm (33.8 in.)

I/O Expansion Cabinet  
width - 62.2 cm (24.5 in.)  
height - 110.5 cm (43.5 in.)  
depth - 85.8 cm (33.8 in.)

Tape Cabinet  
width - 62.2 cm (24.5 in.)  
height - 110 cm (43.5 in.)  
depth - 85.8 cm (33.8 in.)

## Maximum Weight

System Cabinet  
430 kg (950 lbs. max)  
I/O Expansion Cabinet  
450kg (1000 lbs. max)  
Tape Cabinet  
450 kg (1000 lbs. max)

## OPERATING SYSTEM

Concentrix - Berkeley 4.3 UNIX with  
parallel extensions

## PROGRAMMING LANGUAGES

FX/Fortran - ANSI X3.9-1978, with 8X  
extensions  
FX/Ada  
ANSI/MIL-STD-1815-A  
(validated by U.S. DOD)  
FX/C-Draft ANSI X3J11  
Assembler

## APPLICATIONS PACKAGE

More than 200 third party applications

## NETWORK SERVICES

Ethernet  
TCP/IP  
DECnet, DECnet Batch  
Network File System (NFS)  
Network Computing System (NCS)  
Network Queuing System (NQS)  
UltraNet

## VAX/VMS INTEGRATION

FX/Fortran with VAX/VMS extensions  
DCL-like command line interpreter  
EDT+ editor  
DR11W interface support  
DECnet support

## GRAPHIC LIBRARIES

PHIGS/PHIGS+  
X Window System, Version 11

## Corporate Headquarters

Alliant Computer Systems Corporation  
One Monarch Drive  
Littleton, Massachusetts 01460  
508-486-4950 800-622-1113

## European Headquarters

Alliant Computer Systems UK Ltd.  
10 Heatherley Road, Camberley  
Surrey, GU15 3LW  
United Kingdom  
+44 276-682765

## Pacific Rim Headquarters

Nihon Alliant Computer Systems  
Diamond Plaza Building, 25-Ichibancho  
Chiyoda-ku Tokyo 102  
Japan  
03-222-1766

FX/2800 Series, FX/Ada, FX/RT, FX/C, ANSR, FX/Fortran and FX/2800 are trademarks of Alliant Computer Systems. Concentrix is a registered trademark of Alliant Computer Systems. UNIX is a registered trademark of AT&T. Ada is a registered trademark of the U. S. Government (Ada Joint Program Office). Ethernet is a trademark of Xerox Corp., DECnet, VAX, VMS, DCL, Digital Command Language are trademarks of Digital Equipment Corporation, NFS and NQS are trademarks of Sun Microsystems, Inc., NCS and Network Computing System are registered trademarks of Apollo Computer Inc., UltraNet is a registered trademark of Ultra Network Technologies, i860 is a trademark of Intel Corporation., X11 and X Window System, Version 11 are trademark of the Massachusetts Institute of Technology, VISEdge and VIA-CL are trademarks of Visual Edge Software Limited., Cray and UNICOS are trademarks of Cray Research, Inc., MathAdvantage is a registered trademark of Quantitative Technology Corp., IMSL is a trademark of IMSL, Inc.

Alliant has offices in 35 sales and service locations throughout the world. For a list of U.S. or international locations please call Corporate Headquarters.

The materials contained herein are summary in nature, subject to change, and intended for general information only. Details and specifications concerning the use and operation of Alliant equipment and software are available through local sales representatives.

All rights reserved. Printed in U.S.A.

 **ALLIANT**  
Computer Systems Corporation